REMARKS

This Preliminary Amendment is filed in order to facilitate processing of the above-identified application and is filed in response to the Office Action dated July 18, 2006 in which the Examiner rejected claims 1-14 under 35 U.S.C. §103.

As indicated above, claims 1 and 14 have been amended in order to make explicit what is implicit in the claim. The amendment is unrelated to a statutory requirement for patentability.

Claims 1-14 were rejected under 35 U.S.C. §103 as obvious over Synopsys Design Compiler Tools (http://web.archive.org/web/20020814203544/ http://www.synopsys.com/products/logic/design_compiler.html) in view of "*Introduction to ASIC Design Methodology*".

Synopsys merely discloses a device for carrying out a timing verification of a circuit whose design has been completed and after having prepared a description of a Registered Transfer Level (RTL). In particular, *Synopsys* discloses RTL must be input in order to make a logical connection. However, as claimed in claims 1 and 14, the timing information generating apparatus generates timing information on a non-completed functional block whose timing verification has not yet been completed. However, *Synopsys* teaches away from the claimed invention since the device for carrying out timing verification is for a circuit whose design has been completed and described at the RTL. In other words, setting a delay time for a non-completed functional block whose timing verification has not yet been completed cannot be deduced from the design compiler tool of *Synopsys*.

"Introduction to ASIC Design Methodology" discloses post-synthesis simulations to verify the gate level circuit fully provides the desired functionality and

meets the appropriate timing requirements. Thus, nothing in the reference shows, teaches or suggests a timing generating apparatus for generating timing information on a non-completed functional block whose timing verification has not yet been completed as claimed in claims 1 and 14. Rather, the reference merely discloses post-synthesis simulations to meet the appropriate timing requirements.

Furthermore, the reference merely discloses a pre-synthesis simulation to verify the RTL abstraction fully provides the desired functionality and the functional verification of the design that occurs at this point must be as complete and thorough as possible. Thus, the reference clearly teaches away from the claimed invention since the functional verification of the design must be complete. However, as claimed in claims 1 and 14, the timing information generating apparatus generates timing information on a non-completed functional block whose timing verification has not yet been completed.

Since nothing in *Synopsys* or *Introduction* show, teach or suggest a timing information generating apparatus for generating timing information on a non-completed functional block whose timing verification has not yet been completed as claimed in claims 1 and 14, Applicant respectfully requests the Examiner withdraws the rejection to claims 1 and 14 under 35 U.S.C. §103.

Claims 2-13 depend from claim 1 and recite additional features. Applicant respectfully submits that claims 2-13 would not have been obvious over the *Synopsys* website and "*Introduction to ASIC Design Methodology*" within the meaning of 35 U.S.C. §103 at least for the reasons as set forth above. Therefore, applicant respectfully requests the Examiner withdraws the rejection to claims 2-14 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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Date November 17, 2006 By:

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